



Attorney Docket No.: 0254-094-CIP-5

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Title: Low Profile Chip Scale Stacking System and Method
Application No.: 10/631,886
Filing Date: 07/14/2003
Inventor: James W. Cady, et al.
Assignee: Staktek Group, L.P.
Examiner: To Be Assigned
Group: 2831

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Pursuant to the guidelines for Information Disclosure Statements, 37 C.F.R. §§ 1.97-1.98, attached hereto is PTO Form 1449 (nine sheets) with references listed for consideration by the Office.

In accordance with 37 C.F.R. § 1.98(a), copies of the listed written references are being provided.

In accordance with 37 C.F.R. §§ 1.97(g)-(h), the filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made or an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b) or prior art under 35 U.S.C. § § 102 or 103.

This Information Disclosure Statement is being filed before receipt of the first Office action, so no fee is believed to be due. The Commissioner is hereby authorized to charge any fees which may be required in connection with the filing, or to credit any overpayment to Deposit Account No. 50-0897,

upon which account the undersigned has the authority to sign. **A duplicate copy of Form 1449 is enclosed.**

Respectfully submitted,

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February 9, 2004

VIA US MAIL

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Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Re: App No. 10/631,886; "Low Profile Chip Scale Stacking System and Method"
Docket No. 0254-094-CIP-5

Dear Commissioner:

Please find enclosed for filing the following:

1. Information Disclosure Statement;
2. Form 1449 (and one duplicate copy);
3. 142 references; and
4. a return postcard for confirmation of receipt.

The Commissioner is hereby authorized to charge any fees which may be required to Deposit Account 50-0897. Please return the postcard confirming your receipt of the enclosed materials.

Yours truly,

ANDREWS & KURTH LLP

Pam Menke
Board Certified Legal Assistant in Civil Trial Law
Texas Board of Legal Specialization

/pm
enclosures

Form PTO-1449 (Modified
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Patent and Trademark Office**INFORMATION DISCLOSURE STATEMENT BY APPLICANT**

(Use several sheets if necessary)

(37 CFR 1.98(b))

ATTY. DOCKET NO.

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0254-094-CIP-5

10/631,886

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Cady, et al

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GROUP

2818

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	4,763,188	8/9/1988	Johnson, Thomas	357/74		11/4/1987
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						Yes	No
	5-21697(A)	01/1993	Japan			Partial	
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	Dense-Pac Microsystems, 16 Megabit High Speed CMOS SRAM DPS1MX16MKn3
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	"Design Techniques for Ball Grid Arrays," William R. Newberry, Xynetix Design Systems, Inc.
	"Chip Scale Packaging and Redistribution," Paul A. Magill, Glenn A. Rinne, J. Daniel Mis, Wayne C. Machon, Joseph W. Baggs, Unitive Electronics Inc.

EXAMINER

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	6,300,679B1	10/9/2001	Mukerji et al.	257/738		6/1/1998
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						Yes	No
	EP 461-639-A	12/1991	European			X	
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	"Alterable Interposer Block for Personalizing Stacked Module Interconnections," <i>IBM Technical Disclosure Bulletin</i> , Vol. 30, No. 8, January 8, 1988, pp. 373-374.
	IBM Preliminary 168 Pin SDRAM Registered DIMM Functional Description & Timing Diagrams
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	"Tessera Introduces uZ™ - Ball Stacked Memory Package for Computing and Portable Electronic Products" Joyce Smaragdis, Tessera Public Relations; 2 figures that purport to be directed to the uZ™ - Ball Stacked Memory Package.

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	US2002/0139577A1	10/3/2002	Miller, Charles A.	174/261		3/27/2001
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					Yes	No

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	Ron Bauer, Intel. "Stacked-CSP Delivers Flexibility, Reliability, and Space-Saving Capabilities", Spring 2002.
	Tessera uZ Ball Stack Package. 4 figures that purport to be directed to the uZ - Ball Stacked Memory, 1 Page.
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	Flexible Thinking: Examining the Flexible Circuit Tapes. (Website 2 pages) Fjelstad, Joseph.
	Die Products: Ideal IC Packaging for Demanding Applications - Advanced packaging that's no bigger than the die itself brings together high performance and high reliability with small size and low cost. (Website 3 pages with 2 figures) Larry Gilg and Chris Windsor. December 23, 2002.
	Flexible Printed Circuit Technology - A Versatile Interconnection Option. (Website 2 pages) Fjelstad, Joseph. December 3, 2002.

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